**P2 Design Documentation**

Oscar So (ons4) Michael Rigney (mjr372)

**1 Introduction**

The purpose of this document is to understand our design of pipelining a RISC-V CPU on logism. The document will cover an overview of the document, as well as descriptions for each stage in the CPU and also include sub-circuits and testing. This document should provide people, with knowledge of circuits, who view our design a thorough understanding of each stage component.

• Provide references for any other documents, such as textbook, reference manual, etc.

• Define any important terms, acronyms, or abbreviations.

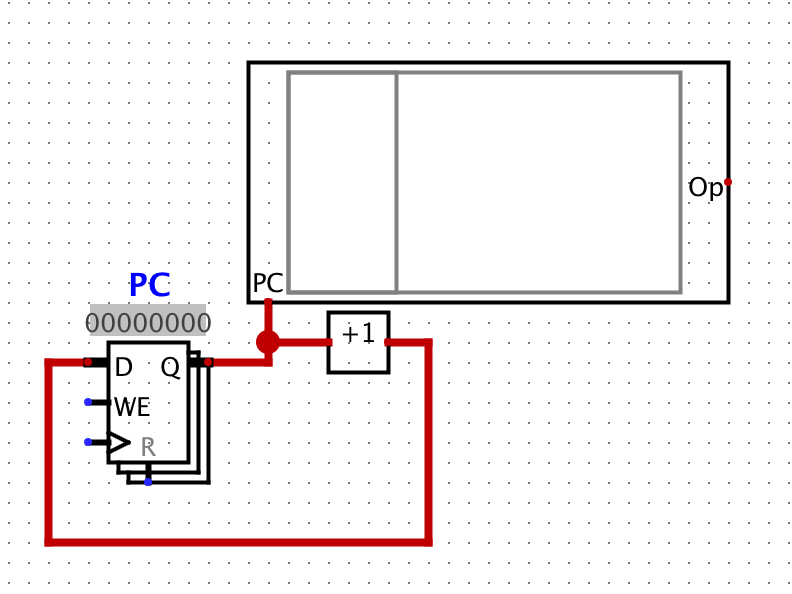
**2 Overview**

The RISC-V CPU that we will be working on is a 5-staged pipelined CPU that takes in operations and executes it to be written in the memory. In simple words, this is the backbone behind simple codes like logical and arithmetic statements.

**3 The Fetch Stage**

3.1 Circuit Diagram

Top level schematic and description



3.2 Correctness Constraints

State the functional requirement of this module.

• item 1

• item 2

• item 3

3.3 Testing

State the approach to verify the functional correctness of this module.

**4 The Decode Stage**

3.1 Circuit Diagram

Top level schematic and description

4.1.1 Submodule A

Submodule A schematic and description

4.1.2 Submodule B

Submodule B schematic and description

4.2 Correctness Constraints

State the functional requirement of this module.

• item 1

• item 2

• item 3

4.3 Testing

State the approach to verify the functional correctness of this module.

**5 The Execute Stage**

5.1 Circuit Diagram

Top level schematic and description

5.1.1 Submodule A

Submodule A schematic and description

5.1.2 Submodule B

Submodule B schematic and description

5.2 Correctness Constraints

State the functional requirement of this module.

• item 1

• item 2

• item 3

5.3 Testing

State the approach to verify the functional correctness of this module.

**6 The Memory Stage**

6.1 Circuit Diagram

Top level schematic and description

6.1.1 Submodule A

Submodule A schematic and description

6.1.2 Submodule B

Submodule B schematic and description

6.2 Correctness Constraints

State the functional requirement of this module.

• item 1

• item 2

• item 3

6.3 Testing

State the approach to verify the functional correctness of this module.

**7 The Writeback Stage**

7.1 Circuit Diagram

Top level schematic and description

7.1.1 Submodule A

Submodule A schematic and description

7.1.2 Submodule B

Submodule B schematic and description

7.2 Correctness Constraints

State the functional requirement of this module.

• item 1

• item 2

• item 3

7.3 Testing

State the approach to verify the functional correctness of this module.